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EXAMINER	
JONES, ERIC W	

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2892	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/582,711	BLANCHARD, PIERRE	
	Examiner	Art Unit	
	ERIC W. JONES	2892	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) *1-15,24 and 26-29* is/are withdrawn from consideration.

5)☒ Claim(s) *31-39* is/are allowed.

6)☒ Claim(s) *16-23 and 25* is/are rejected.

7)☒ Claim(s) *30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 June 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/25/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 16- 21 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al (US 7,101,726 B2) in view of Min (US 7,244,632 B2-prior art of record) and Kirby et al (US 2005/0275049 A1-prior art of record).

Re claim 16, Yamamoto et al disclose in FIGS. 6A-20C a process for the fabrication of contact pads of electronic chips in a semiconductor wafer comprising, on a front face of the wafer, a thin active layer of semiconductor material, the process comprising steps of:

formatting of etched layers (3 in FIG. 11A) on the wafer (21 in FIG. 9B) containing active devices (photodiodes, PD in FIG. 11A); bonding the wafer by its front face onto a support substrate (8 in FIG. 9B); and thereafter thinning down of the semiconductor wafer via a backside opposite the front face (FIG. 10B), depositing at least one metal layer (15 in FIG. 14A) on the backside thus thinned, and etching at least one contact pad (15 in FIG. 16B) in said metal layer, said process including the following steps: etching a narrow trench (FIG. 7C) into the wafer, before the bonding operation, this trench extending into the wafer over a depth approximately equal to the residual semiconductor wafer thickness that will remain after the thinning operation,

filling the space opened by said trench with a conducting material (12/27 in FIG. 12A) isolated from the active devices, thus forming a conducting via between the front face and the backside of the thinned wafer, wherein said trench is a parallel trench located under the contact pad, the contact pad being in electrical contact with the conducting material in said parallel trench. (column 12, lines 40-47,59-67; column 13, lines 1-67)

Yamamoto et al fail to disclose the active layer; etching narrow trenches into the thin active layer; forming conducting vias; and wherein said trenches comprise a series of parallel trenches located under the contact pad, the contact pad being in electrical contact with the conducting material in said parallel trenches.

Min discloses an image sensor comprising an active layer comprising a lightly doped (p-) epitaxial layer (11 in FIG. 4) and etching narrow trenches into the active layer. (column 6, lines 40-62)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the active layer comprising a lightly doped (p-) epitaxial layer of Min with active devices of Yamamoto et al, and to use it and the etching narrow trenches into the active layer with the method of Yamamoto et al to produce an image sensor that easily senses red, green, and blue light via an optical wave within a depletion area. (Min column 3, lines 36-40)

Kirby et al disclose etching narrow trenches (through-wafer interconnects 226 in FIG. 2 and FIG. 6) into the active layer (604); forming conducting vias; and wherein said trenches comprise a series of parallel trenches located under the contact pad (222/224), the contact pad being in electrical contact with the conducting material in said parallel

trenches for use in an image sensor (200 in FIG. 2 and FIG. 6). (¶ [0016]-¶ [0017], ¶ [0025]; ¶ [0054])

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the narrow vertical trenches (through-wafer interconnects) of Kirby et al with method of Yamamoto et al and Min to couple device bond-pads to device ball-pads without mounting the imager to a separate, larger interposer substrate. (Kirby et al, ¶ [0026])

Re claim 17, Yamamoto et al disclose the trench (FIG. 7C) is formed before other deposition and etching steps of electrically functional layers (3 in FIG. 9A) on the front face of the semiconductor wafer (21). (FIGS. 6A-9A; (column 12, lines 40-47, 59-67; column 13, lines 1-67)

Yamamoto et al fail to disclose trenches.

Kirby et al disclose etching narrow trenches (through-wafer interconnects 226 in FIG. 2 and FIG. 6) into the active layer (604); forming conducting vias for use in an image sensor (200 in FIG. 2 and FIG. 6). (¶ [0016]-¶ [0017], ¶ [0025]; ¶ [0054])

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the narrow vertical trenches (through-wafer interconnects) of Kirby et al with method of Yamamoto et al and Min as discussed above for claim 16.

Re claim 18, Yamamoto et al disclose said trench comprises a trench in the form of an alignment marker visible from the backside after thinning in order to allow alignment of the patterns for etching of the layers on the backside with respect to the patterns for etching of layers on the front face. (column 6, lines 23-51)

Yamamoto et al fail to disclose trenches.

Kirby et al disclose etching narrow trenches (through-wafer interconnects 226 in FIG. 2 and FIG. 6) into the active layer (604); forming conducting vias for use in an image sensor (200 in FIG. 2 and FIG. 6). (¶ [0016]-¶ [0017], ¶ [0025]; ¶ [0054])

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the narrow vertical trenches (through-wafer interconnects) of Kirby et al with method of Yamamoto et al and Min as discussed above for claims 16 and 17.

Re claim 19, Yamamoto et al disclose the said at least one metal layer (15 in FIG. 14A) is deposited onto the backside of the wafer (2/21) after thinning, this layer being connected, by conducting a via formed within at least one narrow trench, to at least one conducting layer (11 in FIG. 14A) formed, prior to bonding the wafer onto the support substrate, on the front face of the wafer.

Yamamoto et al fail to disclose conducting vias.

Kirby et al disclose etching narrow trenches (through-wafer interconnects 226 in FIG. 2 and FIG. 6) into the active layer (604); forming conducting vias for use in an image sensor (200 in FIG. 2 and FIG. 6). (¶ [0016]-¶ [0017], ¶ [0025]; ¶ [0054])

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the narrow vertical trenches (through-wafer interconnects) of Kirby et al with method of Yamamoto et al and Min as discussed above for claims 16-18.

Re claim 20, Yamamoto et al disclose said electronic chips comprise at least one image sensor (FIG. 4) with a matrix of pixels (photodiodes, PD in FIG. 8C). (column 12, lines 59-67)

Yamamoto et al fail to disclose the said at least one metal layer comprises a pattern within the matrix of pixels.

Kirby et al disclose one metal layer comprises a pattern (222 or 224 in FIG. 6) within the matrix of pixels (200 in FIG. 6). (¶ [0016]-¶ [0017], ¶ [0025]; ¶ [0054])

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the one metal layer comprising a pattern within the matrix of pixels of Kirby et al with method of Yamamoto et al and Min to form contacts to multiple pixels of a sensor.

Re claim 21, Yamamoto et al disclose layers of color filters (6 in FIG. 15C) are deposited onto the backside of the wafer after bonding and thinning. (column 14, lines 17-19)

Re claim 25, Yamamoto et al and Kirby et al fail to disclose the semiconductor wafer comprises a highly-doped silicon substrate coated with a more lightly doped epitaxial layer forming the active layer, of around 5 to 20 microns thickness, and in that the depth of the trenches is substantially equal to the thickness of the epitaxial layer.

Min discloses an image sensor comprising a highly-doped (p+) silicon substrate (10 in FIG. 4) coated with a more lightly doped (p-) epitaxial layer (11 in FIG. 4) forming the active layer, and forming trenches (41 in FIG. 4) in the active layer. (column 6, lines 40-62)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the highly-doped (p+) silicon substrate coated with a more lightly doped (p-) epitaxial layer forming the active layer of Min with the substrate and active devices of Yamamoto et al, and to use them with the method of Yamamoto et al and Kirby et al to produce an image sensor that easily senses red, green, and blue light via an optical wave within a depletion area. (Min column 3, lines 36-40)

Also, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the active layer, of around 5 to 20 microns thickness, and in that the depth of the trenches is substantially equal to the thickness of the epitaxial layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233. See MPEP § 2144.05.

3. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al and Min and Kirby et al as applied to claim 16 above, and further in view of Pourquier et al (US 7,217,590 B2-prior art of record).

Re claim 22, Yamamoto et al and Kirby et al fail to disclose the semiconductor wafer and its support substrate are bonded onto another, transparent, substrate and the support substrate is eliminated.

Pourquier et al the semiconductor wafer (30 in FIG. 4) and its support substrate (20 in FIG. 4) are bonded onto another, transparent, substrate (80 in FIG. 7) and the support substrate is eliminated. (column 8, lines 33-62; column 9, lines 3-18)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the semiconductor wafer and its support substrate are bonded onto another, transparent, substrate and the support substrate is eliminated of Pourquier et al with the method of Yamamoto et al and Min and Kirby et al to produce connection pads flush with the conductive layers of the imager. (column 9, lines 15-18)

4. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamamoto et al and Min and Kirby et al as applied to claim 16 above, and further in view of Bazan et al (US 6,515,317 B1-prior art of record).

Re claim 23, Yamamoto et al disclose the trench (FIG. 7C) has its internal walls coated with an insulator (SiN 14/26 in FIGS. 8C and 11C) and is filled with a metal (12/27 in FIGS. 11C and 12A). (column 12, lines 40-55; column 13, lines 48-67)

Yamamoto et al and Min and Kirby et al fail to disclose a thin silicon oxide and highly doped polycrystalline silicon.

Bazan et al disclose trenches (FIG. 6) have their internal walls coated with thin (500 Å) silicon oxide (16 in FIG. 7 by thermal oxidation of silicon substrate) and are filled with polycrystalline silicon (7 in FIG. 7) that is highly doped ($1x10^{19}$ atoms/cm^3) so as to be conducting. (column 4, lines 26-40, 48-53, 65-67; column 5, lines 1-2; column 6, lines 31-34: claim 8)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to substitute the thin silicon oxide and polycrystalline silicon that is highly doped so as to be conducting of Bazan et al with the insulation and metal of

Yamamoto et al, and to use it with the method of Yamamoto et al and Min and Kirby et al to produce highly conductive interconnects.

Allowable Subject Matter

5. Claim 30 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 31-39 are allowed over the prior art of record.

The following is a statement of reasons for the indication of allowable subject matter: Re claim 31, the prior art of record cannot be used singularly nor in combination to satisfy the claimed limitations of: the contact pad being electrically connected through said semiconductor region to at least one conductive layer formed during said step of formatting, and the contact pad being isolated from the conductive material filling said continuous trench.

The applicant has disclosed that such a configuration as formed by the claimed method is distinct from prior art references.

Re claims 32-39, they are allowable because of their dependence on claim 31.

Response to Arguments

7. Applicant's arguments with respect to claims 16-25 have been considered but are moot in view of the new ground(s) of rejection in view of Yamamoto et al (US 7,101,726 B2) and Min (US 7,244,632 B2-prior art of record) and Kirby et al (US 2005/0275049 A1-prior art of record) and Pourquier et al (US 7,217,590 B2-prior art of record) and Bazan et al (US 6,515,317 B1-prior art of record).

8. In regards to applicant's argument that Yamamoto et al and Kirby et al do not suggest ***'narrow trenches'***.

The examiner takes the position that both Yamamoto et al and Kirby et al do, indeed, suggest narrow trenches when the trenches are viewed compared to the substrates in which they are formed. In the case of Yamamoto et al, in FIG. 7C the width of the trench is narrow compared to the substrate (21) width. Such is the case for Kirby et al as well when the width of trenches 226 in FIGS. 2 and 6 are compared to the substrate in which they are formed.

Further, narrow is a relative term which suggests variation or degree of a dimension(s) when compared to another dimension(s). Also, the applicant has not claimed what constitutes narrow.

Therefore, in view of the width of the trenches compared to the width of the substrates of both Yamamoto et al and Kirby et al, and the fact that the applicant has not claimed what constitutes narrow, the limitations of the claims are satisfied.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC W. JONES whose telephone number is (571)270-3416. The examiner can normally be reached on Monday-Friday 5:30AM-3:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thao X. Le can be reached on (571)272-1708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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2/12/2009